

FLOORPLAN EVALUATION, GLOBAL ROUTING,
AND BUFFER INSERTION FOR INTEGRATED CIRCUITS

ABSTRACT OF THE DISCLOSURE

A method and system for evaluating a floorplan and for defining a global buffered routing for an integrated circuit including constructing a graphical representation of the integrated circuit floorplan, including wire capacity and
5 buffer capacity; formulating an integer linear program from said graphical representation; finding a solution to said integer linear program.